ABSTRACT

This invention relates to matched instruction set processor systems and a method, system, and apparatus to efficiently design and implement matched instruction set processor systems by mapping system designs to re-configurable hardware platforms. The method includes decomposing the matched instruction set processor system into interconnected design vectors, each of the interconnected design vectors including a binding header method, a run method, a conjugate virtual machine (CVM), a binding trailer method, and an invocation method. The method also includes analyzing and mapping the interconnected design vectors into a re-configurable platform.